REMARKS

This application has been carefully reviewed in light of the Examiner's Action dated September 30, 2005. Claims 1-25 remain as originally presented. New Claims 26-30 have been added. Reconsideration of full allowance is respectfully requested.

Initially, Applicant notes with appreciation the Examiner's indication that Claims 13-25 are allowed and that Claims 2, 6 and 7 include allowable subject matter. As Applicant believes that all of the Claims are allowable for the reasons set forth below, Claims 2, 6 and 7 have not been re-written in independent form at this time.

In the Examiner's Action, the Examiner rejected Claims 1, 3-5, 8-10 under 35 U.S.C. § 103 as being unpatentable over Shor et al (United States Patent No. 6,035,001) in view of Lee (United States Patent No. 6,790,685). This rejection is respectively traversed for reasons set forth below.

Independent Claim 1 is directed to a method for precisely etching a wide bandgap semiconductor device. More specifically, the method of Claim 1 involves providing a multi-layer laminate including at least a first and second layer of wide bandgap semiconductor material, isolating an area of the first layer of semiconductor material for locating a conductance measurement device, measuring a first conductance of the isolated area of the first layer of semiconductor material using the conductance measurement device, first etching a first amount of the first layer of semiconductor material, measuring a second conductance of the isolated area of the first layer of semiconductor material subsequent to etching the first amount of the first layer of semiconductor material, and utilizing the first and second measured conductance to determine a time required to etch a second amount of the first layer of semiconductor material. As set forth in the specification, isolating an area of interest for locating a conductance

measurement device allows for a more accurate conductance measurement by minimizing current leakage and the influence of other features such as emitter mesas in close proximity and/or defects in the semiconductor material. A more accurate conductance measurement allows for determination of a more precise time required to etch a desired amount of the first layer of semiconductor material. This improved method of constructing wide bandgap semiconductor devices addresses the need for careful control of layer thicknesses in semiconductor devices and also addresses the necessity of precision etching in fabricating wide bandgap semiconductor devices.

The Examiner cites Shor as "utilizing the first and second measured conductance to determine the dwell time/a time required to etch a second amount of the first layer of semiconductor material." The method in Shor does not disclose or suggest the use of a measured conductance to determine the dwell time. The dwell time in Shor is "calculated by dividing the spot size by the scan speed." (col 6, lines 9-10) In any event, the method in Shor does not disclose or suggest the use of a measured conductance to determine an etch time. Shor is directed at a "method for selective conductivity etching." Shor discloses that the n-type layer is biased at a potential such that the "n-type SiC layer will photo-corrode and the p-type SiC layer will be inert and act as an etch stop" (emphasis added). Due to the etch stop layer disclosed in Shor, it is not necessary to determine a precise time required for etching. In Shor, once the etching reaches the etch stop layer, the etching will stop and the material can remain in the etching solution and no more etching will take place. Accordingly, Shor does not address the same problems associated with the need for careful control of layer thicknesses or the need for precision etching in fabricating wide bandgap semiconductor devices. It is therefore unsurprising

that Shor fails to suggest or disclose using first and second conductance measurements of an isolated area to determine an etch time.

Lee, as the Examiner notes, "discloses a method for forming a test pattern compris[ing] the step of measuring a voltage/conductance of the isolated area of the semiconductor material using a measuring line/conductance measuring device." However, Lee is directed to "a method of forming a test pattern in a semiconductor device which can identify overetch and underetch that occur side walls [sic] of a pattern after an etching process is disclosed," and to "an etching profile of the under layer to which an etching process is performed...." (emphasis added) More specifically, Lee addresses issues associated with isotropic and non-vertical etching and does not address the problem of controlling layer thicknesses. Accordingly, Lee fails to suggest or disclose a method for determining an etch time much less using first and second conductance measurements of an isolated area to determine an etch time.

Thus, even if they could be properly combined, Shor and Lee do not disclose or suggest a method for using first and second conductance measurements of an isolated area to determine an etch time. Furthermore, Applicant respectfully submits that it is not proper to combine Shor and Lee because Shor addresses a method for selective conductivity etching and Lee addresses a method of identifying issues with isotropic and non-vertical etching. Thus, there is no suggestion or motivation to combine Shor and Lee as the Examiner has proposed. Accordingly, for all of the foregoing reasons, it is submitted that this rejection is improper and should be withdrawn.

In addition, the Examiner rejected Claims 11-12 under 35 U.S.C. § 103 as being unpatentable over Shor et al (United States Patent No. 6,035,001) in view of Lee (United States Patent No. 6,790,685) and further in view of Temple (US 4,314,266). This rejection is respectively traversed for reasons set forth below.

As noted above, Shor and Lee fail to disclose or suggest a method of using a first and second measured conductance of an isolated area to determine an etch time. Temple does not supply such disclosure, and it is therefore submitted that the proposed combination does not yield the claimed subject matter. Furthermore, Temple fails to disclose or suggest a method for etching a wide bandgap semiconductor device such as a transistor or a thyristor. As the Examiner noted, Temple discloses a method of forming a thyristor having a PN junction, however, Temple notes in the specification that a foundation semiconductor body in a thyristor device is "typically formed of monocrystalline silicon processed to provide a PNP structure...." Thus, Temple fails to disclose or suggest that the thyristor or transistor device can be formed from silicon carbide or from a wide bandgap semiconductor material.

Moreover, Applicant respectfully submits that it would not be proper, as Examiner suggests, to combine Shor in view of Lee and further in view of Temple. Because of the different material properties of monocrystalline silicon and wide bandgap semiconductor materials such as silicon carbide, the two types of semiconductors are not substitutable. Moreover, Temple does not address the etching of a wide bandgap semiconductor device such as a thyristor or transistor and does not address any of the differences between the practical issues associated with the fabrication processes of monocrystalline silicon and wide bandgap semiconductors such as silicon carbide.

For all of the foregoing reasons, Applicant respectfully submits that Claims 11-12 are patentable over the proposed combination of Shor, Lee and Temple, and this rejection should be withdrawn.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation

would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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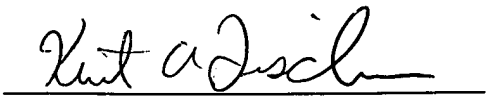
By: 

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